UDC 621.396.962.25 DOI: 10.18698/0236-3933-2019-3-95-102

CHANGING THE DELAY OF THE ANALOG-DIGITAL CONVERSION IN REDUCE THE LEAKAGE SIGNAL EFFECT

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Abstract

The research of reduction the leakage signal effect in short range radiolocation system is considered. LFM signal is used as a probe signal. The structure of the differential frequency signal and the structure of operating harmonic are shown for the spectral method of processing the useful signal. To reduce the leakage signal effect, it is proposed to use subsampling of the useful signal with a variable delay of the clock signal of the analog-to-digital converter. The dependence between the level of the parasitic component of the operating harmonic signal, due to the leakage signal effect, and the delay of the clock signal of the analog-digital converter, is given. The clock signal of the analog-digital converter is generated by a microcontroller timer. The timer is initialized in pulse width modulation mode. The required delay of the clock signal of the analog-digital converter is selected by changing the threshold of the timer. For testing the algorithm, a microwave module *K-LC5* and a prototype board with a microcontroller *STM32F407* are used

Keywords

Short range radiolocation system, microwave module, linear frequency modulation, difference frequency signal, subsampling, leakage signal effect, microcontroller

Received 15.01.2019

Introduction. Modern, radiolocation systems are increasingly finding the use of short range microwave modules of the 24, 60 and 120 GHz bands [1–5]. They are used in automotive systems [6, 7], remote vital signs monitors [8, 9] and security systems [10]. They usually include: a voltage controlled oscillator (VCO), which allows the use of an arbitrary modulation of the signal; transmitting and receiving antennas; low noise amplifier (LNA); mixer. A modulated voltage is applied to the input of such a microwave module, and an intermediate frequency signal is generated at its output.

Microwave modules have small dimensions, so the distance between the transmitting and receiving antennas is small (about a centimeter). Consequently, the isolation between the antennas is weak and the leakage signal can significantly exceed the useful signal reflected from the target. Thus, when developing a system, especially when operating at short distances, it is necessary to take into account the effects of a leakage signal.

As a modulating voltage $u_m(t)$, an unbalanced ramp signal, linear frequency modulation (LFM) is widely used [11–14]. This achieves high resolution in range and speed with a fairly simple implementation.

The purpose of the work is to reduce the influence of the leakage signal in a small-sized microwave module, using LFM.

The relationship between the level of the component of the working harmonic signal, due to the leakage signal effect, and the delay of the clock pulse signal of the analog-to-digital converter. When using asymmetric LFM, the difference frequency signal represents the sum of the useful and parasitic components [15]. The useful component is due to reflection from a moving target, and the parasitic component is due to leakage signal and reflection from fixed objects

$$e(t) = E_u \sum_{n=0}^{\infty} A_{un} \cos\left[2\pi(nF_m + F_D)t + \Phi_{un}\right] + \\ + E_p \sum_{n=1}^{\infty} A_{pn} \cos\left(2\pi n F_m t + \Phi_{pn}\right),$$

where E_u, E_p are the amplitudes of the useful and parasitic components; A_{un}, A_{pn} are amplitudes of the n-th harmonic; F_m is modulation frequency; F_D is Doppler frequency; Φ_{un}, Φ_{pn} are initial phases of the n-th harmonic.

With the spectral processing method, working harmonics are distinguished from the difference frequency signal using band-pass filters

$$e_n(t) = E_u A_{un} \cos\left[2\pi(nF_m + F_D)t + \Phi_{un}\right] + E_p A_{pn} \cos\left(2\pi n F_m t + \Phi_{pn}\right).$$

Subsampling is applied in the Ref. [16] to combat the leakage signal effect. The signal $e_n(t)$ is digitized with a sampling rate F_s, satisfying the conditions $F_s > 2F_D$ and $F_s = F_m/N$, where N is a positive integer. Thus, at the output of the analog-to-digital converter (ADC), we get

$$u_n(k) = U_{un} \cos\left(2\pi F_D \frac{k}{F_s} + \varphi_{un}\right) + U_{pn} \cos\left(\varphi_{pn}\right). \quad (1)$$

Here, U_{un}, U_{pn} are the amplitudes of the useful and parasitic component of the signal at the output of the ADC; k is the ADC report number $(k = tF_s)$;

φ_{un}, φ_{pn} are the initial phases of the useful and parasitic component of the signal at the output of the ADC.

The constant component $u_n(k)$, caused by the leakage signal effect, can be suppressed with a high-pass filter (HPF). However, if the Doppler frequency F_D is small, an HPF is required with a steep characteristic. It is difficult to implement such an HPF with limited computational resources; therefore, in this paper, we propose another approach to eliminate the parasitic constant component.

The value of the initial phase of the parasitic component of the signal at the ADC output φ_{un} depends on the initial phase of the parasitic component of the difference frequency signal Φ_{pn} and on the delay τ_s of the ADC clock signal $u_s(t)$ (Fig. 1):

$$\varphi_{pn} = \Phi_{pn} - \tau_s \frac{nF_m}{F_s}. \tag{2}$$

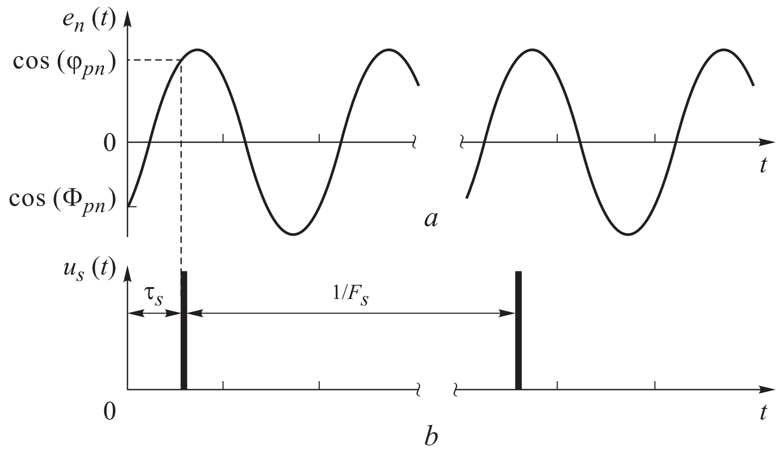

Fig. 1. Diagrams of signals $e_n(t)$ (*a*) and $u_s(t)$ (*b*) with single amplitudes

Substituting (2) into (1), we obtain the dependence of the level of the parasitic component of the signal on the ADC output $u_n(k)$ on the delay τ_s of the ADC clock signal $u_s(t)$:

$$u_n(k) = U_{un} \cos\left(2\pi F_D \frac{k}{F_s} + \varphi_{un}\right) + U_{pn} \cos\left(\Phi_{pn} - \tau_s \frac{nF_m}{F_s}\right). \tag{3}$$

By adjusting the delay value τ_s so that the second term of expression (3) equals zero, one can eliminate the influence of the leakage signal effect. It should be noted that the initial phase Φ_{pn} at each turn on of the microwave module is randomly the value, but during the operation of the module does not change. Therefore, each time the device is turned on, the delay value τ_s of the ADC clock signal $u_s(t)$ must be calculated again.

Implementation of the algorithm for selecting the delay of the clock signal of the analog-digital converter. The clock signal of the ADC $u_s(t)$ with variable delay τ_s can be generated using a microcontroller timer. The timer should be initialized in the pulse-width modulation (PWM) mode (Fig. 2).

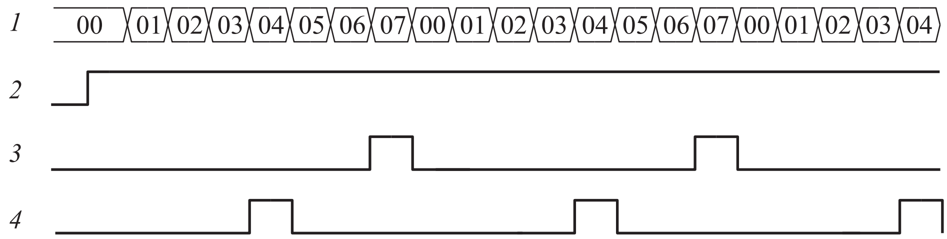

Fig. 2. Timer operation in PWM mode, the base of the count is 7:
1 is timer counter value; *2* is timer operation enable signal; *3* is PWM signal, *CCR* = 7;
4 is PWM signal, *CCR* = 4

By changing the value in the CCR comparison register (see Fig. 2); you can adjust the delay τ_s of the ADC clock signal $u_s(t)$.

For testing the algorithm for selecting the ADC clock delay value, the microwave module K-LC5 and the prototype board with the *STM32F407* microcontroller are used. The following peripherals are involved in the microcontroller: a phase locked loop system (PLL, input frequency multiplier); ADC; timer; DAC (Fig. 3).

The microcontroller is clocked from the quartz oscillator G1 with the frequency F_{clk}. of the PLL increases the frequency of the quartz oscillator by an integer number of times: $F_{PLL} = MF_{clk}$. The output signal from the PLL is used to clock the timer and the digital synthesizer G2 signal. A digital signal synthesizer generates a modulating voltage $u_m(t)$, namely, an asymmetrical ramp signal with a frequency F_m, of multiple frequency F_{PLL}.

The modulating voltage $u_m(t)$ is applied to the VCO. The LFM oscillation is emitted by the transmit antenna A_{tx}. The reflected signal enters the receiving antenna A_{rx}, amplifies in the LNA and is mixed with a part of the emitted oscillation. At the output of the microwave module, a differential frequency signal $e(t)$ is generated. Then the band-pass filter (BPF) selects the working harmonic $e_n(t)$, which is fed to the input of the ADC. In turn, the ADC starts the conversion by the clock signal $u_s(t)$ from the timer output.

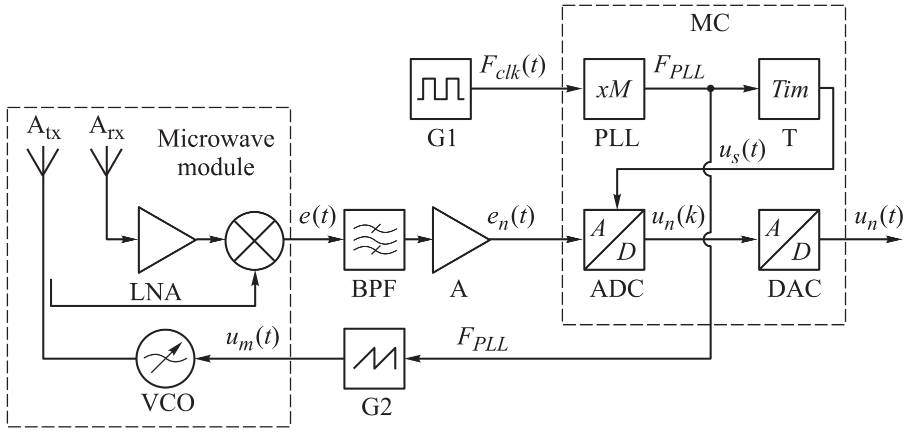

Fig. 3. Block diagram for the implementation of the algorithm for selecting the delay value of the ADC clock signal:

A_{tx}, A_{rx} are transmitting and receiving antennas; G1 is a quartz crystal controlled oscillator of the clock signal; G2 is digital signal oscillator (arbitrary waveform generator); BPF — BandPass Filter; A — amplifier; T — timer; MC — microcontroller; DAC — Digital to Analog Converter

The timer operates in PWM mode. The basis of the count is chosen so that the PWM frequency $F_s = F_m / N$.

Consider the algorithm for selecting the ADC clock delay value.

1. When the device is turned on, the value of the *CCR* comparison register in the timer changes step by step from the minimum to maximum value (the minimum value is zero and the maximum value is based on the timer count).

2. At each step, the value of the constant component at the output of the ADC and the corresponding value of the comparison register *CCR* are recorded.

3. From the received array, the value of the *CCR* comparison register is selected, which corresponds to the minimum value of the constant component.

4. The device starts to work in normal mode with the new value of the register of comparison *CCR*.

To test the algorithm, the signal from the ADC output $u_n(k)$ is fed directly to the DAC. The signal from the output of the DAC $u_n(t)$ is controlled by an oscilloscope. If the constant component is suppressed by the proposed algorithm, then the signal $u_n(t)$ will be equal to $u_n(t) = V_{ref}/2$, where V_{ref} is the reference voltage of the DAC (on this prototype board $V_{ref} = 3.3$ V, $V_{ref}/2 = 1.65$ V). If there is a constant component from the leakage signal, the signal $u_n(t)$ will be shifted relative to $V_{ref}/2$. The signals from the DAC output $u_n(t)$ at different initial phases of the leakage signal shown in Fig. 4.

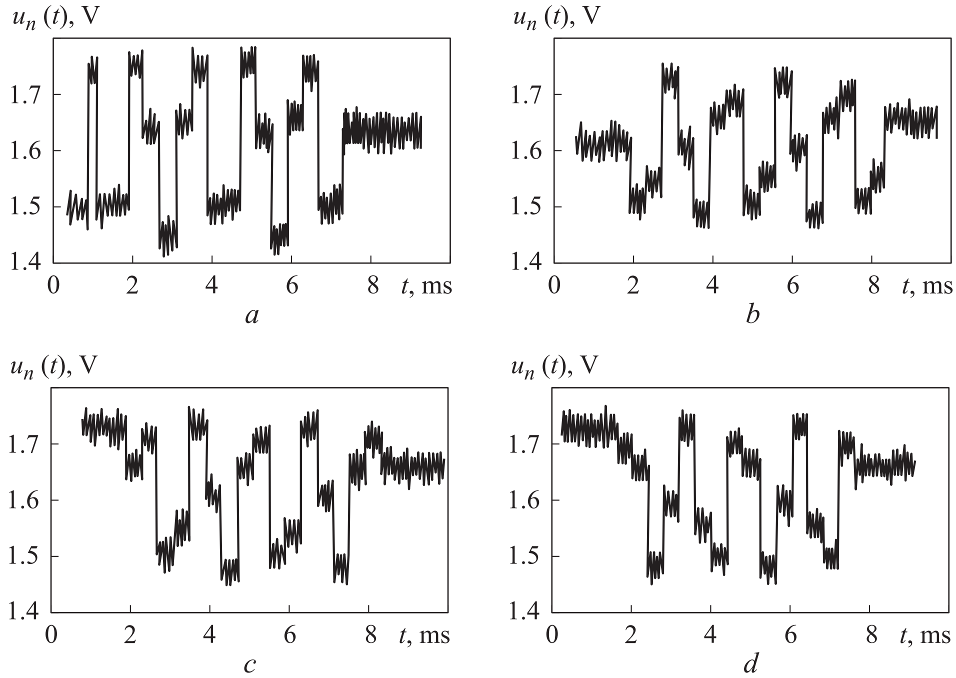

Fig. 4. Signals from the output of the DAC $u_n(t)$ at various initial phases of the leakage signal:
a, b are $u_n(t) < V_{ref}/2$; *c, d* are $u_n(t) > V_{ref}/2$

At the initial time, a parasitic constant component is present in the signal from the output of the ADC $u_n(k)$, due to the leakage signal, and each time the device is turned on, its value is different. For signals in Fig. 4, *a* and *b* $u_n(t) < V_{ref}/2$, for signals in Fig. 4, *c* and *d* $u_n(t) > V_{ref}/2$. During the operation of the algorithm, the value of the delay signal of the ADC clock signal and, accordingly, the level of the parasitic component change. After the completion of the algorithm, a delay is chosen at which $u_n(k) \to 0$, $u_n(t) \to V_{ref}/2$. So the influence of the leakage signal effect is reduced.

Conclusions. The use subsampling of the harmonic signal of the difference frequency with a variable delay of the ADC clock signal allows to reduce the effect of the leakage signal. In the proposed implementation of the algorithm, there is no high-pass filter after the ADC, which allows the use of near-location systems for detecting signals with a low Doppler frequency value.

When processing multiple harmonics of a differential frequency signal (multichannel system), it is necessary to take into account that the phases of the parasitic components for each operating harmonic are different, therefore, for each channel there must be a different delay value of the ADC clock signal. In this case, several microcontroller timers are used, one per channel. The basis of the counting of timers is set the same, and the value of the register of comparison is selected individually for each channel.

The main requirement when using subsampling: synchronization of the modulating voltage and the ADC clock signal. In the proposed implementation, it is accomplished through the use of a microcontroller PLL system. It clocks both the digital signal synthesizer, which generates the modulating voltage, and the timer, which generates the ADC clock signal.

Translated by A. Rozhok

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Please cite this article as:

Kichigin A.A., Shakhtarin B.I. Changing the delay of the analog-digital conversion in reduce the leakage signal effect. *Herald of the Bauman Moscow State Technical University, Series Instrument Engineering*, 2019, no. 3, pp. 95–102.
DOI: 10.18698/0236-3933-2019-3-95-102

Издательство МГТУ им. Н.Э. Баумана
105005, Москва, 2-я Бауманская ул., д. 5, стр. 1
press@bmstu.ru www.baumanpress.ru

Подписано в печать 10.06.2019
Формат 70 × 108/16
Усл.-печ. л. 9,0

Отпечатано в типографии МГТУ им. Н.Э. Баумана
105005, Москва, 2-я Бауманская ул., д. 5, стр. 1
baumanprint@gmail.com